

CLAIMS

What is claimed is:

1. A graphics accelerator, comprising:
 - 2 a plurality of specialized processing subunits, interconnected through a serial message-passing interface to provide a generally pipelined graphics accelerator architecture; and
 - 5 a memory interface which provides a high bandwidth interface directly to a local buffer associated with said graphics accelerator.
- 1 2. The accelerator of Claim 1, wherein ones of said subunits are 3 configured so that said memory interface accesses multiple tiles of pixels simultaneously.
- 1 3. A graphics accelerator, comprising:
 - 2 a plurality of specialized processing subunits,
 - 3 interconnected through a serial message-passing interface to 4 provide a reconfigurably pipelined graphics accelerator 5 architecture;
 - 6 at least one of said specialized processing subunits comprising 7 multiple subprocessors connected to operate in parallel on 8 separate tasks; and
 - 9 a high bandwidth memory interface which interfaces to a local 10 buffer of said graphics accelerator;
 - 11 wherein said serial interface also permits downloading of image data 12 to ones of said subunits.

- 1 4. The accelerator of Claim 1, wherein ones of said subunits are
2 configured so that said memory interface accesses multiple tiles
3 of pixels simultaneously.